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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/729,010	12/04/2000	Michael Ficco	PD-200235	6750

7590 02/12/2004

Hughes Electronics Corporation
Patent Docket Administration
P.O. Box 956
Bldg. 1, Mail Stop A109
El Segundo, CA 90245-0956

EXAMINER	
HOFFMAN, BRANDON S	
ART UNIT	**PAPER NUMBER**
2136	5

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/729,010	FICCO, MICHAEL	
	Examiner	Art Unit	
	Brandon Hoffman	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-9,12,17-20,33,37-42,44,48-51 and 54-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-9,12,17-20,33,37-42,44,48-51 and 54-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1, 5-9, 12, 17-20, 33, 37-42, 44, 48-51, and 54-62 are pending in this office action, claims 54-62 are newly added.

2. Applicant's arguments filed January 23, 2004, with respect to claims 6-9, 17-20, 38-41, 48-51, 55-57, and 60-62 have been considered but are moot in view of the new ground(s) of rejection.

Rejections

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

4. Claims 1, 5, 12, 33, 37, 42, 44, 54, and 59 are rejected under 35 U.S.C. 102(a/b/e) as being anticipated by Tsukamoto et al (U.S. Patent No. 5,796,828).

Regarding claims 1, 33, and 44, Tsukamoto et al. teaches a method/apparatus for storing and retrieving digital data within a hardware platform (figure 2), the method comprising:

- Receiving data bits across a bus, the data bits forming a bit pattern (figure 2, reference numbers 103 and 20);
- Altering the bit pattern of the data bits (figure 2, reference number 22);

- Storing the altered data bits (figure 2, reference numbers 23A, 24, and 40);
- Restoring the altered data bits to the bit pattern (figure 2, reference number 25); and
- Outputting the restored data bits (figure 2, reference numbers 26 and 105),
    - Wherein the altering comprises one of selectively inverting bits in selected bit positions of the data bits and selectively scrambling bits in the selected bit positions of the data bits to prevent unauthorized use of the data bits (the encipherer 22 performs these steps as indicated in the examiners 'Response to Arguments').

Regarding claim 33, specifically, Tsukamoto et al. teaches a computer-readable medium for carrying one or more sequences of one or more instructions for storing and retrieving digital video data within a hardware platform (figure 2, reference number 104A, and column 5, lines 40-52), the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform the steps stated in claims 1 and 44, as mentioned above.

Regarding claim 5 and 37, Tsukamoto et al. teaches wherein the altering step and the restoring step are performed by a hard disk drive interface (figure 2, reference number 23A).

Regarding claim 12, Tsukamoto et al. teaches an apparatus for storing and retrieving digital video data (figure 2), comprising:

- A system bus configured to transfer data bits, the data bits forming a bit pattern (figure 2, reference numbers 103, 20 and 21A);
- An interface coupled to the system bus and configured to alter the bit pattern of the data bits (figure 2, reference numbers 22, 23A, and 25); and
- A hard disk drive coupled to the interface and configured to store the altered data bits (figure 2, reference number 40),
    - Wherein the interface is configured to alter the bit pattern by one of selectively inverting bits in selected bit positions of the data bits and selectively scrambling bits in the selected bit positions of the data bits to prevent unauthorized use of the data bits (the encipherer 22 performs these steps as indicated in the examiners 'Response to Arguments').

Regarding claim 42, Tsukamoto et al. teaches wherein the altered data bits are stored on a hard disk drive (column 4, lines 19-28).

Regarding claims 54 and 59, Tsukamoto et al. teaches a method for storing and retrieving digital data within a hardware platform (figure 2), the method comprising:

- Receiving a plurality of data bits, the data bits forming a bit pattern (figure 2, reference numbers 103 and 20);

- Altering the bit pattern by inverting bits in a first selection of bit positions of the data bits/scrambling bits of selected but positions of the data bits (figure 2, reference number 22, the encipherer 22 performs these steps as indicated in the examiners 'Response to Arguments');
- Storing the altered bit pattern on a medium (col. 4, lines 19-21);
- Retrieving the stored altered bit pattern from the medium (col. 4, lines 21-24);
- Restoring the altered bit pattern by inverting the bits of the first selection of bit positions of the retrieved bit pattern/unscrambling the bits of the selected bit positions of the retrieved bit pattern (figure 2, reference number 25, the decipherer 25 performs these steps as indicated in the examiners 'Response to Arguments'); and
- Outputting the restored data bits (figure 2, reference numbers 26 and 105).

Claim Rejections - 35 USC § 103

5. Claims 6-9, 17-20, 38-41, 48-51, 55-57, and 60-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto et al (U.S. Patent No. 5,796,828) in view of Armbruster et al. (U.S. Patent No. 5,208,853).

Regarding claims 6, 7, 17, 18, 38, 39, 48, 49, 55, and 60, Tsukamoto et al. teaches all the limitations of claims 1, 12, 33, 44, 54, and 59, respectively, above. However, Tsukamoto et al. does not teach wherein the altering is unique to the hardware platform/plurality of platforms.

Armbruster et al. teaches wherein the altering is unique to the hardware platform/plurality of platforms (col. 4, lines 45-64, by using the serial number of a device for altering, wherein the serial number is unique (or at least relatively unique), the altering will be unique to each device, and therefore unique to the hardware platform.).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine altering is unique to the hardware platform/plurality of platforms, as taught by Armbruster et al., with the method/apparatus or Tsukamoto et al. It would have been obvious to one of ordinary skill in the art to combine altering is unique to the hardware platform/plurality of platforms, as taught by Armbruster et al., with the method/apparatus of Tsukamoto et al. because the uniqueness of each platform provides a new alteration for each platform, therefore hindering a hacker from successfully retrieving content from other hardware platforms if one particular platform were to be compromised.

Regarding claims 8, 19, 40, 50, 56, and 61, Tsukamoto et al. teaches all the limitations of claims 1, 12, 33, 44, 54, and 59, respectively, above. However, Tsukamoto et al. does not teach wherein the altering is based upon a serial number of the hardware platform.

Armbruster et al. teaches wherein the altering is based upon a serial number of the hardware platform (col. 4, lines 45-64).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine altering based upon a serial number of the hardware platform, as taught by Armbruster et al., with the method/apparatus or Tsukamoto et al. It would have been obvious to one of ordinary skill in the art to combine altering based upon a serial number of the hardware platform, as taught by Armbruster et al., with the method/apparatus of Tsukamoto et al. because the serial number provides a unique/relatively unique number to allow certain systems to receive updates of altered data (col. 2, lines 7-19).

Regarding claims 9, 20, 41 51, 57, and 62, Tsukamoto et al. teaches all the limitations of claims 1, 12, 33, 44, 54, and 59, respectively, above. However, Tsukamoto et al. does not teach (a processor coupled to the system bus for) generating a random number upon power-up of the hardware platform, wherein the altering is based upon the random number.

Armbruster et al. teaches (a processor coupled to the system bus for) generating a random number upon power-up of the hardware platform, wherein the altering is based upon the random number (col. 3, lines 3-29).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine altering based upon the random number, as taught by Armbruster et al., with the method/apparatus or Tsukamoto et al. It would have been

obvious to one of ordinary skill in the art to combine altering based upon the random number, as taught by Armbruster et al., with the method/apparatus of Tsukamoto et al. because the random number provides a secure way to alter data based on a string of numbers that a potential interceptor would not be able to figure out.

Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto et al (U.S. Patent No. 5,796,828) in view of Gannett (U.S. Patent No. 3,944,745).

Regarding claim 58, Tsukamoto et al. teaches all the limitations of claim 54, above. However, Tsukamoto et al. does not teach wherein the altering further comprises scrambling bits of a second selection of bit positions of the bit pattern, and the restoring further comprises unscrambling the bits of the second selection of bit positions of the retrieved altered bit pattern.

Gannett teaches wherein the altering further comprises scrambling bits of a second selection of bit positions of the bit pattern (fig. 7A), and the restoring further comprises unscrambling the bits of the second selection of bit positions of the retrieved altered bit pattern (fig. 7B).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine scrambling bits of a second selection of bit positions

and unscrambling bits of the second selection, as taught by Gannett, with the method or Tsukamoto et al. It would have been obvious to one of ordinary skill in the art to combine scrambling bits of a second selection of bit positions and unscrambling bits of the second selection, as taught by Gannett, with the method of Tsukamoto et al. because a second round of scrambling will provide even more security.

Response to Arguments

6. Applicant amends claims 1, 6-9, 12, 17-20, 33, 38-42, 44, and 48-51, and adds claims 54-62.

7. Applicant argues:

a. Independent claims 1, 12, 33, and 44 are not taught by Tsukamoto et al. to include "selectively inverting bits in selected bit positions of the data bits and selectively scrambling bits in the selected bit positions of the data bits to prevent unauthorized use of the data bits" (page 14, third full paragraph).

b. Dependent claims 5, 37, and 42 are allowable based upon their dependency on allowable claims 1 and 33 (page 15, first paragraph).

c. Claims 6, 7, 17, 18, 38, 39, 48, and 49 are not taught by Tsukamoto et al. to include "the altering being unique/relatively unique to the hardware platform" (page 15, second paragraph).

d. Claims 8, 19, 40, and 50 are not taught by Tsukamoto et al. to include "the altering is based upon a serial number of the hardware platform" (page 15, last paragraph).

e. Claims 9, 20, 41, and 51 are not taught by Tsukamoto et al. to include "the altering based upon a random number" (page 16, second paragraph).

Regarding argument (a), examiner disagrees with applicant. Tsukamoto et al. discloses an encipherer that utilizes a key, as is well known in the art. Enciphering and deciphering, with the use of a key, inverts selected bits of a data stream. Although the user of the system does not know the exact bits that are inverted/scrambled, the hardware performing the enciphering knows which bits to invert/scramble based on the key used. In other words, the encipherer of Tsukamoto et al. does disclose selectively inverting/scrambling bits in selected bit positions of the data bits to prevent unauthorized use of the data bits from the discretion of the key.

Regarding argument (b), examiner disagrees with applicant. Based on the argument set forth by the examiner for argument (a), the dependent claims stand as rejected.

Regarding argument (c), (d), and (e), examiner agrees with applicant that the Tsukamoto et al. reference does not teach the altering is unique to the hardware platform, the altering is based upon the serial number of the hardware platform, or the altering is based upon a random number. However, the methods used to alter the data, i.e., random numbers and serial numbers of the hardware, are very well known methods. Both numbers provide very random, very unique numbers that would prevent an interceptor (hacker) from breaking into the system to steal content. By using the random, unique numbers, even if a hacker were to intercept content on one device, the

method to intercept content on another device would be totally different, thus preventing the stealing of content.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon Hoffman whose telephone number is 703-305-4662. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 703-305-9648. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Brandon Hoffman

BH
2/5/04

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100